TONE\_CTRL IP SPEC

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## Introduction

The TONE\_CTRL module is used to generate tones.

## Feature

Key features of the TONE\_CTRL module are:

•All functions are for both AFE and bridge application

•Generate WAKEUP TONE when received WAKE\_TONE\_DET or WAKE\_TONE\_GEN high.

•Generate STA TONE when received STA\_TONE\_DET or when STA\_TONE\_GEN high.

•Generate SD TONE on N port after SD\_TONE\_GEN high. Direction in TONE\_TRANS\_EN shall base on SPI\_DIR.

•Generate FLT TONE on N port every 50ms when SLEEP high and FLT\_WAKE high.

•Generate HB TONE on N port every 400ms when SLEEP high and FLT\_WAKE low.

•TONE transmitting and daisy chain transmitting are mutually exclusive.

•WAKE TONE and STA TONE shall have higher priority to HB TONE and FLT TONE.

## Register Definition

### Register Map

Table 1 TONE\_CTRL Register Map

| **Name** | **Add** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Default** |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| CTRL1 | 0x2002 | SOFT\_RSTB | DIR\_SEL |  | WAKE\_TONE\_GEN | STA\_TONE\_GEN | SD\_TONE\_GEN | TO\_SD | TO\_SLEEP | 0x80 |
| CTRL2 | 0x2003 |  |  |  |  |  | CMP\_BIST\_GO | ADD\_W\_EN | SPI\_DIR | 0x00 |

## Functional Details

### Block Diagram

The following diagram shows the TONE\_CTRL architecture and internal modules and connections.



Figure 1 TONE\_CTRL diagram

### Module input/output list

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Dir | Width | Discirption | duration |
| D2A\_CLR\_WAKEUP | O | 1 | Pulse for analog to clear A2D\_WAKE\_UP\_x | 1 CLK\_256K |
| clr\_WAKE\_TONE\_GEN | O | 1 | Pulse for module u\_COMM\_REG to clear WAKE\_TONE\_GEN | 1 CLK\_256K |
| clr\_STA\_TONE\_GEN | O | 1 | Pulse for module u\_COMM\_REG to clear STA\_TONE\_GEN | 1 CLK\_256K |
| pos\_HBFSAT | O | 1 | HB too fast condition is detected | 1 CLK\_256K |
| pos\_HBTO | O | 1 | HB too slow(timeout) condition is detected | 1 CLK\_256K |
| TONE\_TRANS\_EN\_N | O | 1 | N port tone transmission enable | Level(CLK\_OUT domain) |
| TONE\_TRANS\_EN\_S | O | 1 | S port tone transmission enable | Level(CLK\_OUT domain) |
| TONE\_CLK | O | 1 | Tone clock | 1 CLK\_256K |
| TONE\_POLAR | O | 1 | Tone polar(1: positive tone; 2: negative tone) | Level(CLK\_256K domain) |
| rx\_en\_256K | O | 1 | Synchronoused rx\_en\_ds\_or\_spi by CLK\_256K | Level(CLK\_256K domain) |
| SLEEP\_MODE | O | 1 | Synchronoused A2D\_SLEEP\_1P8 by CLK\_256K | Level(CLK\_256K domain) |
| SD\_TONE\_GEN\_EN | O | 1 |  |  |
| clr\_SD\_TONE\_GEN | O | 1 | Pulse for module u\_COMM\_REG to clear SD\_TONE\_GEN | 1 CLK\_256K |
| CLK\_256K\_SC | I | 1 | Scan-muxed CLK\_256K | 50% duty |
| resetb\_CLK\_256K | I | 1 | Asynchronous reset signal(synchronously released by CLK\_256K) | Level(CLK\_256K domain) |
| SOFT\_RSTB | I | 1 | Soft reset | Level(CLK\_SLOW domain) |
| CLK\_OUT\_SC | I | 1 | CLK\_OUT after scan mux |  |
| resetb\_SR\_CLK\_OUT | I | 1 | Asynchronous reset signal (synchronously released by CLK\_OUT) and SOFT\_RSTB logic | Level(CLK\_OUT domain) |
| A2D\_WAKE\_UP\_N | I | 1 | Wake tone detected from N port | async |
| A2D\_WAKE\_UP\_S | I | 1 | Wake tone detected from S port | async |
| A2D\_STA\_DET\_N | I | 1 | STA tone detected from N port | async |
| A2D\_STA\_DET\_S | I | 1 | STA tone detected from S port | async |
| HB\_TONE\_DET | I | 1 | Heart beat tone detected | async |
| D2A\_RX\_EN\_S | I | 1 | enable daisy chain receiving on S port | Level(CLK\_32M domain) |
| D2A\_RX\_EN\_N | I | 1 | enable daisy chain receiving on N port | Level(CLK\_32M domain) |
| WAKE\_TONE\_GEN | I | 1 | Register bit from u\_COMM\_REG to generate wake tone | Level(CLK\_REG domain) |
| STA\_TONE\_GEN | I | 1 | Register bit from u\_COMM\_REG to generate sleep to active tone | Level(CLK\_REG domain) |
| A2D\_SLEEP\_1P8 | I | 1 | Sleep mode indication | async |
| SD\_TONE\_GEN | I | 1 | Register bit from u\_COMM\_REG to generate shut down tone | Level(CLK\_REG domain) |
| SPI\_EN | I | 1 | Enable SPI | Async |
| SPI\_DIR | I | 1 | "1" for north interface, "0" for south interface | Level(CLK\_REG domain) |
| SPI\_RX\_EN | I | 1 | Indicate RX\_DATA\_SPI is update | 1 CLK\_REG |
| rx\_en | I | 1 | daisy chain signal is being received | Level(CLK\_32M domain) |
| tx\_en\_32M | I | 1 |  |  |
| state\_rx\_init | I | 1 | state is STATE\_INIT | 1 CLK\_REG |
| state\_rx\_bps | I | 1 | state is STATE\_BYPASS | 1 CLK\_REG |
| FLT\_WAKE | I | 1 | Indicate fault status | Level(CLK\_SLOW domain) |

#### Clock Domain

The clock for TONE\_CTRL is CLK\_256K\_SC and CLK\_OUT\_SC.

For TONE\_TRANS\_EN\_X related logics, CLK\_OUT\_SC is used.

For others, CLK\_256K\_SC is used.

### TONE\_CTRL function description

TONE\_CTRL module is a sub module in COMM\_DIG. It generates 5 kinds of tones. The 5 tones are described in Table2 and From2.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **PARAMETER** | **SYMBOL** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS** |
| Time between pulses of COMM tones  COMM tones: WAKE, STA, SHUTDOWN | tCOMMTONE |  |  | 11 | 15 | us |
| HIGH time of each pulse of COMM tone | tCOMMTONE\_HI |  | 0.92 | 1 | 1.08 | us |
| LOW time of each pulse of COMM tone | tCOMMTONE\_LO |  | 0.92 | 1 | 1.08 | us |
| Time between pulses of FAULT tones | tFLTTONE |  |  | 11.5 |  | us |
| HIGH time of each pulse of FAULT tone | tFLTTONE\_HI |  |  | 1 |  | us |
| LOW time of each pulse of FAULT tone | tFLTTONE\_LO |  |  | 1 |  | us |
| Time between pulses of HB tones | tHBTONE |  |  | 11.5 |  | us |
| HIGH time of each pulse of HB tone | tHBTONE\_HI |  |  | 1 |  | us |
| LOW time of each pulse of HB tone | tHBTONE\_LO |  |  | 1 |  | us |
| Period between HB tone burst | tHB\_PERIOD |  | 360 | 400 | 440 | ms |
| Timeout to not receive HB | tHB\_TIMEOUT |  | 0.9 | 1 | 1.1 | s |
| Time to receive HB too fast | tHB\_FAST |  |  | 200 |  | ms |
| Period between FAULT tone burst | tFLT\_PERIOD |  |  | 50 |  | ms |
| FAULT tone latency in stack devices | tFLTS\_LATENCY | From time a device receives the tone to the time the same device detects and generates its fault tone |  | 48 |  | us |
| FAULT tone latency in base device | tFLTB\_LATENCY | From time a device receives the tone to the time the same device detects and asserts fault pin |  | 24 |  | us |

Table2 timing requirement for tones

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| WAKE tone | | | STA tone | | | SHUTDOWN tone | | | HB tone | | | FT tone | | |
| n | nDET | Polar | n | nDET | Polar | n | nDET | Polar | n | nDET | Polar | n | nDET | Polar |
| 90 | 60 | + | 30 | 20 | + | 270 | 180 | - | 30 | 20 | - | 90 | 60 | - |

Table3 Numbers and Polarity of Tones

In CLK\_256K domain, 1 clock is 3.9us, so 1us width pulses will be generated in analog part. In digital part, all tones are generated on outputs TONE\_CLK, TONE\_POLAR, TONE\_TRANS\_EN\_N, TONE\_TRANS\_EN\_S.

TONE\_CLK: (HWR001/003/004/005/006\_TONE\_CTRL)

If a tone is being generated, TONE\_CLK is always 1 clock high with 3 clocks period(HWR007\_TONE\_CTRL). After the corresponding numbers of pulses(in Table3) are sent, TONE\_CLK stops toggling.

TONE\_POLAR:

According to Table3, when sending WAKE tone or STA tone, TONE\_POLAR is high. When sending other tones, TONE\_POLAR is low.

TONE\_TRANS\_EN\_N:

When sending tone because of analog detected tones on S port(HWR002\_TONE\_CTRL) (A2D\_WAKE\_UP\_S(HWR001\_TONE\_CTRL) or A2D\_STA\_DET\_S(HWR003\_TONE\_CTRL)), TONE\_TRANS\_EN\_N is high to deliver the tone.

When sending WAKE(HWR012\_TONE\_CTRL) tone, STA(HWR014\_TONE\_CTRL) tone or SHUTDOWN(HWR004\_TONE\_CTRL) tone because of corresponding register bit X\_GEN, if SPI\_DIR is low, TONE\_TRANS\_EN\_N is high.

When sending HB(HWR006\_TONE\_CTRL) tone or FLT(HWR005\_TONE\_CTRL) tone, TONE\_TRANS\_EN\_N is high. HB tone is sent when SLEEP\_MODE high and FLT\_WAKE low, FLT tone is sent when SLEEP high and FLT\_WAKE high(HWR009\_TONE\_CTRL). If SLEEP\_MODE changes to active mode(A2D\_SLEEP\_1P8 changes to high), BM20A response to A2D\_WAKE\_UP\_N/A2D\_WAKE\_UP\_S/A2D\_STA\_DET\_N/A2D\_STA\_DET\_S immediately. (HWR011\_TONE\_CTRL)

As daisy chain transmitting are always start after receiving(copy or response), TONE\_TRANS\_EN\_N changes to 0 when daisy chain starts receiving(HWR010\_TONE\_CTRL).

TONE\_TRANS\_EN\_S:

When sending tone because of analog detected tones on N(HWR002\_TONE\_CTRL) port(A2D\_WAKE\_UP\_N(HWR001\_TONE\_CTRL) or A2D\_STA\_DET\_N(HWR003\_TONE\_CTRL)), TONE\_TRANS\_EN\_S is high to deliver the tone.

When sending WAKE(HWR012\_TONE\_CTRL) tone, STA(HWR014\_TONE\_CTRL) tone or SHUTDOWN(HWR004\_TONE\_CTRL) tone because of corresponding register bit X\_GEN, if SPI\_DIR is high, TONE\_TRANS\_EN\_S is high.

As daisy chain transmitting are always start after receiving(copy or response), TONE\_TRANS\_EN\_N changes to 0 when daisy chain starts receiving(HWR010\_TONE\_CTRL).

Clr\_xxx(xxx is SD\_TONE\_GEN, WAKE\_TONE\_GEN, STA\_TONE\_GEN) is generated after synchronizing the tone source to clear the tone starting state.(HWR008/013/015\_TONE\_CTRL). (Refer to Figure2)

Specially, D2A\_CLR\_WAKEUP is high after the corresponding numbers of pulses (in Table3) are sent(HWR016\_TONE\_CTRL). (Refer to Figure3)



Figure2 WAKE\_TONE\_GEN is written high



Figure3 receive A2D\_WAKE\_UP\_S